IN THE CLAIMS:

1. (currently amended) A computer system comprising:

at least two processing sets, each ~~of which includes~~processing set including a main memory;~~,~~ and

a bridge connecting the processing sets,

wherein at least a first processing set further ~~including~~includes a dirty memory having dirty indicators for indicating dirtied blocks of the main memory of the first processing set, and

wherein the bridge includes a direct memory access controller that is operable to respond to a fault state by controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

2. (original) The computer system of claim 1, wherein the direct memory access controller is operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

3. (original) The computer system of claim 1, wherein the dirty memory comprises control logic operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

4. (original) The computer system of claim 3, wherein the control logic is operable to output references to the dirtied blocks of the main memory to be copied.

5. (original) The computer system of claim 4, wherein the control logic is operable to buffer references to the dirtied blocks of the main memory to be copied.

6. (original) The computer system of claim 4, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

7. (original) The computer system of claim 1, wherein a block of main memory is a page of main memory.

8. (original) The computer system of claim 1, wherein each dirty indicator comprises a single bit.

9. (original) The computer system of claim 1, wherein the direct memory access controller is operable to instigate a search of the dirty memory for dirty indicators indicative of dirtied blocks.

10. (original) The computer system of claim 1, wherein each processing set includes a dirty memory.

11. (original) The computer system of claim 1, wherein the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.

12. (currently amended) A method ~~of~~ for reintegrating the main memory of a computer system comprising:

at least two processing sets, each ~~of which includes~~processing set including a main memory;~~,~~ and

a bridge connecting the processing sets,

the method comprising:

recording an indicator of a block of the main memory of a first processing set that has been dirtied in a dirty memory in the first processing set; and

a direct memory access controller in the bridge responding to a fault state by controlling the copying of blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

13. (original) The method of claim 12, wherein the direct memory access controller searches the dirty memory for dirty indicators indicative of dirtied blocks.

14. (original) The method of claim 12, wherein dirty memory control logic searches the dirty memory for dirty indicators indicative of dirtied blocks.

15. (original) The method of claim 14, wherein the control logic outputs references to the dirtied blocks of the main memory to be copied.

16. (original) The method of claim 15, wherein the control logic buffers references to the dirtied blocks of the main memory to be copied.

17. (original) The method of claim 15, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

18. (original) The method of claim 12, wherein a block of main memory is a page of main memory.

19. (original) The method of claim 12, wherein each dirty indicator comprises a single bit.

20. (original) The method of claim 12, wherein the direct memory access controller instigates a search of the dirty memory for dirty indicators indicative of dirtied blocks.

21. (original) The method of claim 12, wherein the processing sets are operable in lockstep, the method comprising attempting to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.